WHERE INNOVATION BEGINS

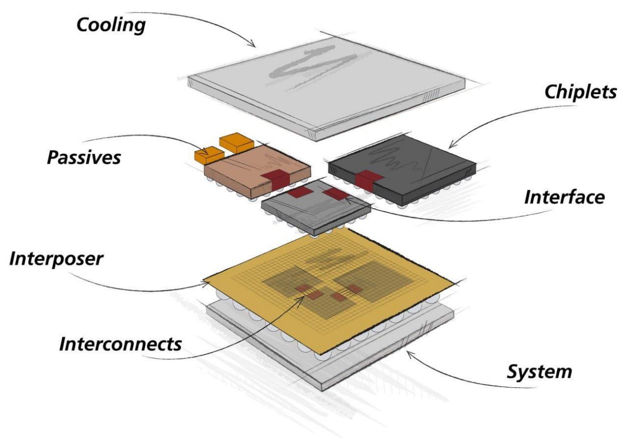
DESIGN AUTOMATION CONFERENCE

Fraunhofer IIS

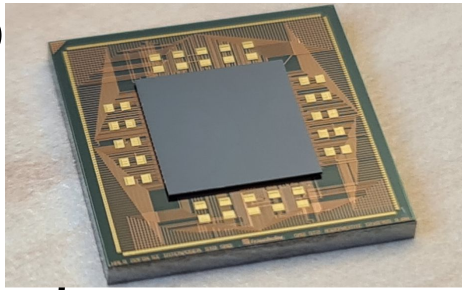
Automatic Chiplet Interface IP Generation Across Technology Nodes, Vendors, and Stacks Using Intelligent IP

Benjamin Prautsch, Andy Heinig

Why Chiplets? What's (one of) the Challenge(s)?

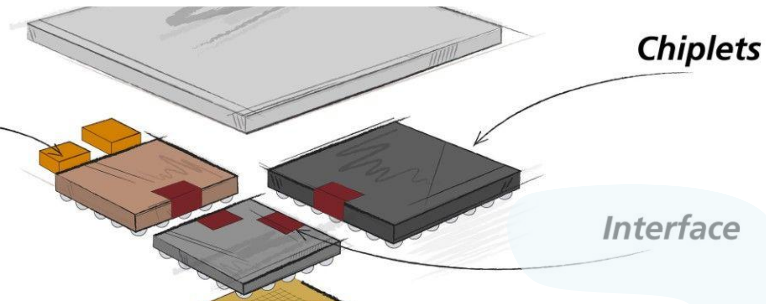


- Disaggregation of functionality into smaller basic blo
  - Standardized interface □ combination of different functionality into new system
  - System is defined on package level by combination of different Chiplets
  - Reuse of basic blocks possible in terms of configurability/adap
  - Second source easier possible



- Different chip technologies possible (processor, analog, …)
- Challenge of Interoperability: Design and Reuse of Interface IP across all necessary Technology Nodes and Metal Stacks

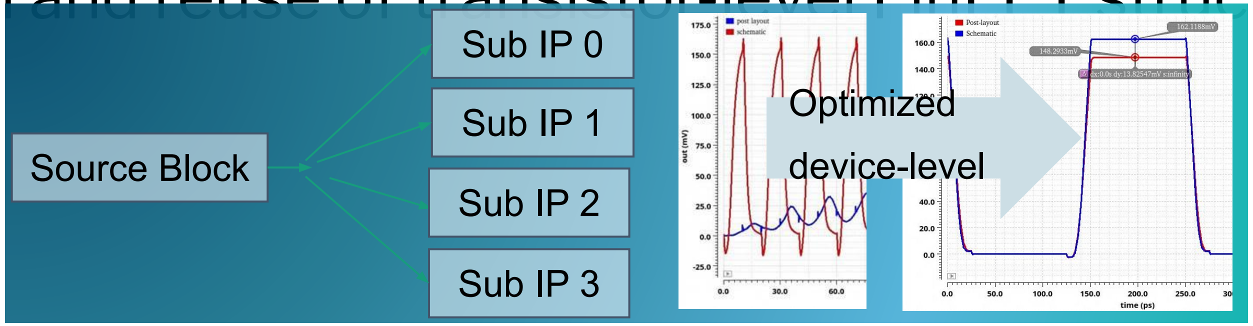
Approach to Chiplet Interface IP: Meet Standards



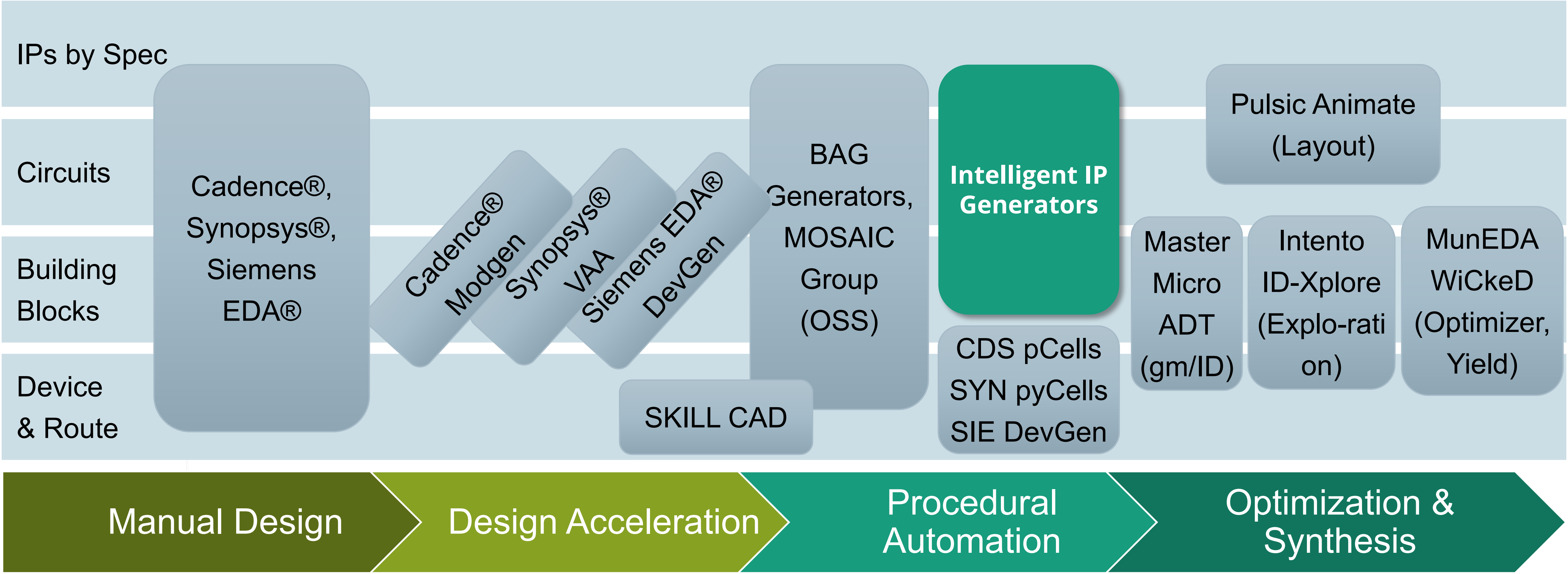
	Bunch of Wires (BoW)	Universal Chiplet Interconnect Express (UCIe)	High Bandwidth Memory (HBM)
Spec	Open Domain Specific Architecture (ODSA)		Established standard
	Version 1.0 available		Version 2.0 available
	16 lines at 16Gbit/s (double data rate)	16 lines at up to 32Gbit/s or 64 lines at up to 32Gbit/s (double data rate)	1024 lines at 2Gbit/s (double data rate)
	Definition of electrical interface		
	No definition of high level protocols	high level protocols – CXI, PCIe	Definition of high level protocols
Pro	Laminate-based Chiplet technology possible	Laminate-based and silicon interposer-based Chiplet technology possible	Very high performance
			Can also be used as standard for processor-processor communication
Con	Limited scaling – based on laminate substrates	Multiple sub-standards (package, protocol)	Silicon Interposer technology necessary
		Different implementations of a Chiplet IP is possible – contradict the idea of Chiplets	

Reuse and Automatic Design Generation Divide and Conquer

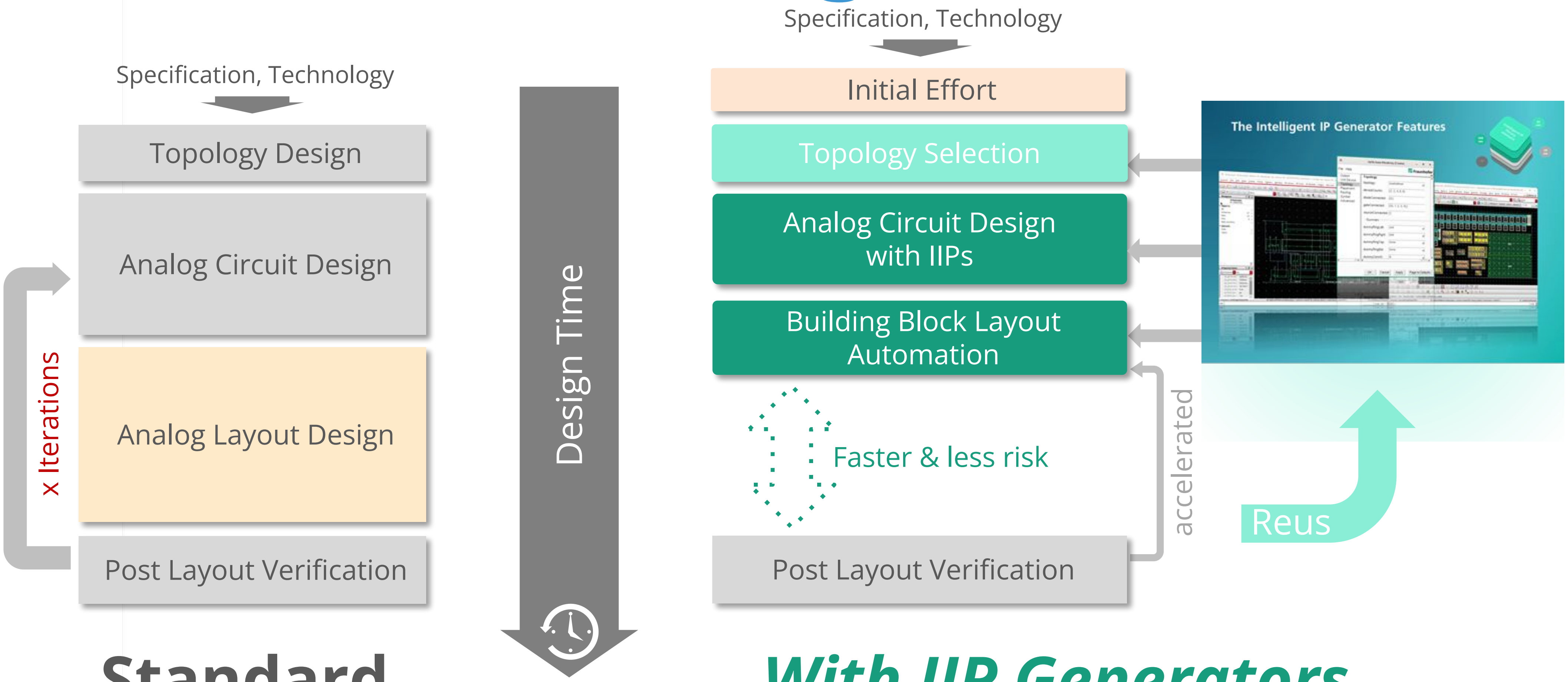
- Use well-defined Chiplet interface (here: BoW @ 5nm Samsung)
    - See https://www.eas.iis.fraunhofer.de/en/media_press/press_releases/pr_20221110_EN.html
- Flexible System Composition
    - Hierarchical & scalable design on architecture level
    - Reuse of transistor-level building blocks
    - Optimization and reuse of transistor-level FinFET structures



Reuse and Automatic Design Generation Automation Levels



Reuse and Automatic Design Generation Automation with Intelligent IP



Standard

With IIP Generators

Reuse and Automatic Design Generation

- Increased Level of Design Automation for Reuse
  - Utilization of complex PDK pCells & SKILL SKILL
  - Utilization of Cadence® ModGen & Mosaic
  - Utilization of our own tool **Intelligent IP (IIP)** (IIP)
    - *Programmatic* Generator-based Automation
    - Support across *various PDKs, vendors, nodes & stacks*
    - *High Flexibility* on Schematic-level & Layout-Level
    - *Fully flow-compatible*
    - *Custom Automation* of interface IP and other IP
- Design strategy of this BoW IP: heavily gridded P&R + “golden” reference

Reuse and Automatic Design Generation

- Utilization of complex PDK pCells & SKILL
  - Automation of device level
  - Automation of parts of the local routing

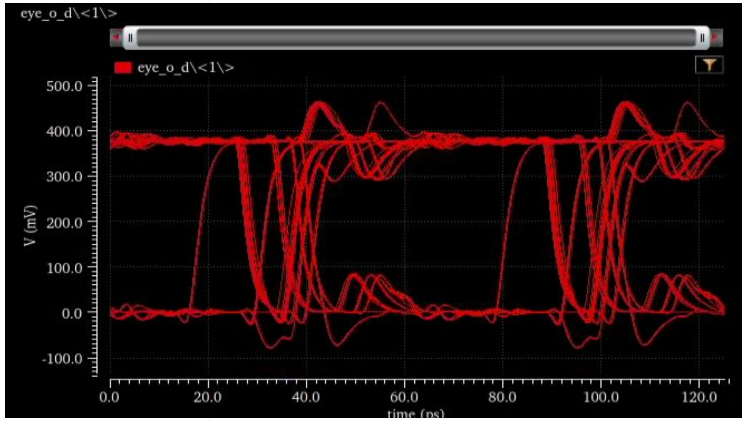
- Utilization of Cadence® ModGen & Mosaic
  - Automation of grids of similar devices and connections, e.g. device multipliers
  - Automation of default routing tracks

- Utilization of our own tool **Intelligent IP (IIP)**
  - Automation of symbol, schematic, and layout
  - Persistent cells are generated into the design library
  - Manual post editing possible if required
  - Full-custom possible

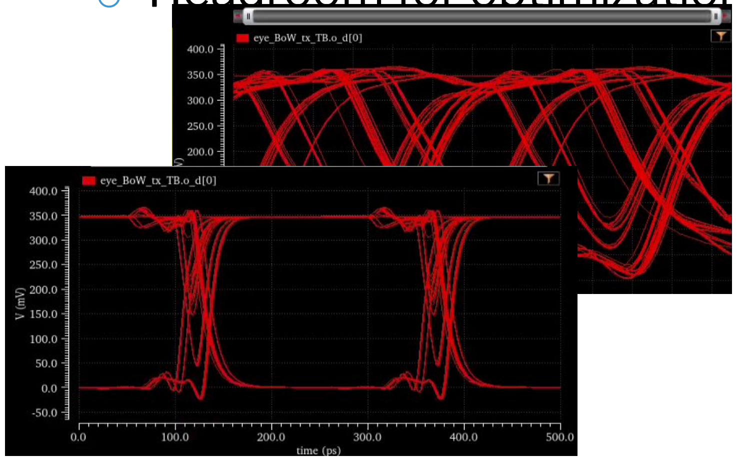
- Key aspect: design expert and EDA expert must identify the automation sweet spots

Simulation Results with Post-Layout Netlist and Silicon Photograph

- Schematic-Level Simulation
  - Static pseudo-random pattern, 255 inputs
  - Highest selected frequency

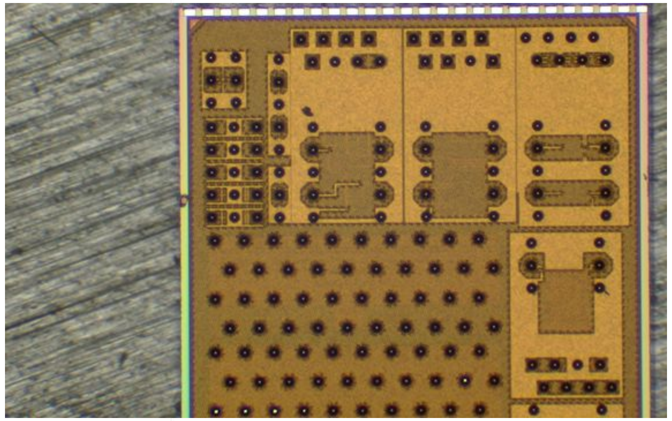


- Layout-Level Simulation
  - Static pseudo-random pattern, 255 inputs
  - Medium to highest selected frequency
  - Headroom for optimization in routing

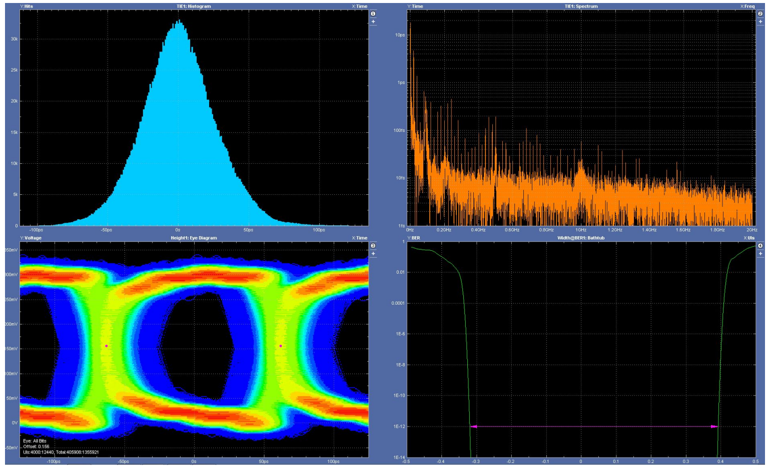


Simulation Results with Post-Layout Netlist and Silicon Photograph

- Chip Photograph
  - Ready for measurement
  - Ready for packaging



- Lab Measurements
  - Measurements ongoing
  - Ready for packaging



Conclusion and Outlook

- Chiplets will be Key Drivers to Enable Cutting-Edge Electronics
  - Enables combination of various IPs and IP types into a single module
  - Enables low-cost modules through mass production of Chiplets
- Take-up of Chiplets will Heavily Rely on Design Eco-System for Interface IP
  - Design Eco-system is key enabler of Chiplets as it enables Chiplet-to-Chiplet communication
  - Standardization activities must be considered: interoperable IP essential for variety of Chiplets
  - Reuse-oriented Interface IP development is key for high variety of Interface IPs
    - Reuse of the architecture / reuse of building blocks
    - Automation to ease reuse cross-Vendor / cross-Technology / cross-Specification
- Chiplet Interface IP Generation is Now Available: It Enables Reuse & Interoperability

Thank You for Your Attention!

- Your Contacts

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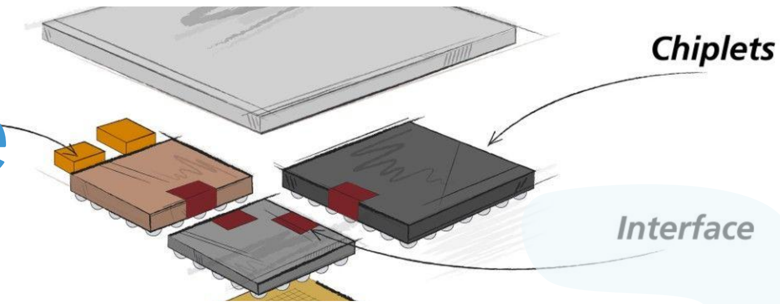
Approach to Chiplet Interface IP: Meet Standards



- Bunch of Wires (BoW)
  - Open Domain Specific Architecture (ODSA)
  - Version 1.0 available
  - 16 lines at 16Gbit/s (double data rate)
  - Definition of electrical interface
  - No definition of high level protocols

Advantage

  - Laminate-based Chiplet technology possible

Disadvantage

  - Limited scaling – based on laminate substrates

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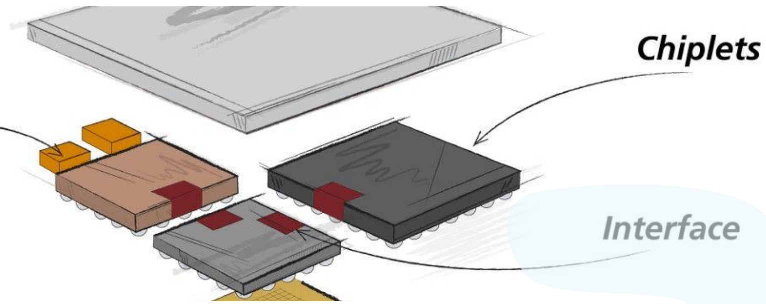

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    - high level protocols – CXI, PCIe

Advantage

- Laminate-based and silicon interposer-based Chiplet technology possible

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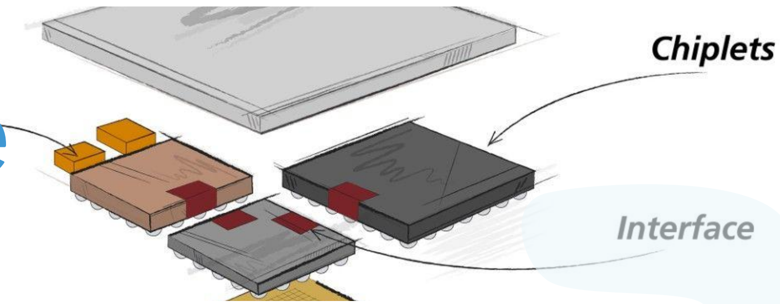

- High Bandwidth Memory (HBM)
    - Established standard
    - Version 2.0 available
    - 1024 lines at 2Gbit/s (double data rate)
    - Definition of electrical interface
    - Definition of high level protocols

Advantage

- Very high performance
- Can also be used as standard for processor-processor communication

Disadvantage

- Silicon Interposer technology necessary